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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,095	10/17/2003	Tomokazu Otani	67162-026	9067
7590 09/23/2004 McDERMOTT, WILL & EMERY 600 13th Street, N.W. Washington, DC 20005-3096			EXAMINER PAREKH, NITIN	
			ART UNIT 2811	PAPER NUMBER

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/687,095	Applicant(s) OTANI ET AL.	
	Examiner Nitin Parekh	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 10 March 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) 5 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 and 3 is/are rejected.
- 7) ☒ Claim(s) 2 and 4 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 October 2003 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>4</u> . | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

1. Applicant's election without traverse of Embodiment I, claims 1-4 in Paper No. 3 is acknowledged.

#### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (US Pat. 6242285).

Regarding claim 1, Kang teaches a stacked semiconductor device (Fig. 4A-4D) comprising:

- a plurality of integrated circuit (IC) packages/semiconductor IC elements (ICE) (see IC-A and IC-B in Fig. 4A-4D) each having a plurality of arranged pads (see 219B on IC-B in Fig. 4D), the ICEs being stacked and housed in the stacked semiconductor device
- an electrical connection lead bar/frame having a bar shape (see 419B in Fig. 4D and 4B) and supplies desired chip selection (CS) function and electrical

connection to the two ICEs depending on particular application requirements

(Col. 7, lines 1-30)

(Fig. 4A-4D; Col. 6, line 35- Col. 7, line 30; Col. 3-7).

Kang fails to explicitly teach the bar shaped frame/connection lead being a power supply bar supplying a power voltage.

Kang further teaches the leads being supplied to perform conventional power or data//input-output (I/O) functions (Col. 10, lines 23-27).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the bar shaped frame/connection lead being a power supply bar supplying the power voltage so that the desired power lead configuration and selection of remaining/other leads such as ground or I/O can be achieved in Kang's stacked device.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (US Pat. 6242285) in view of Oguchi et al. (US Pat. 5332922).

Regarding claim 3, Kang teaches substantially the entire claimed structure as applied to claim 1 above, except the power supply frame being provided on a larger semiconductor element of the two semiconductor elements.

Oguchi et al. teach a stacked device having a plurality of ICE having different sizes (see 1A/1B in Fig. 25) where a leadframe provided on a larger ICE (see 1A in Fig. 25), the leadframe further providing wire bonding connections between the larger ICE and a smaller ICE (see 3A1, 1A, 1B and 5 in Fig. 25; Col. 18, line 56- Col. 19, line 3).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the power supply frame being provided on the larger semiconductor element of the two semiconductor elements as taught by Oguchi et al. so that bonding wire length can be reduced and resin sealing can be improved in Kang's stacked device.

#### ***Allowable Subject Matter***

5. Claims 2 and 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Reasons for Allowance***

6. The following is an examiner's statement of reasons for allowance:

The references of record do not teach either singularly or in combination at least the limitations "wherein the power supply frame is provided on each of the semiconductor elements to which a power supplied, and the power supply frame includes frame portions placed along rows of pads of the semiconductor elements and a

portion coupling the frame portions" or "wherein the power supply frame placed between the rows of the pads of the two semiconductor elements" in a stacked device having the power supply frame providing the power to at least two of the semiconductor elements.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

09-12-04



NITIN PAREKH

PATENT EXAMINER

Technology Center 2800